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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/730,055	DEAS ET AL.	
	Examiner	Art Unit	
	ADOLF DSOUZA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 9, 11 - 14, 17 - 30, 35 - 39, 41 - 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 4, 6 - 9, 11 - 14, 17 - 21, 35 - 39, 41 - 45* is/are rejected.

7)☒ Claim(s) *5, 22 – 30, 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/30/2009 has been entered.

Response to Arguments

2. Applicant's response to the 35 USC 101 rejection has been accepted by the Examiner.

3. Applicant's arguments with respect to claim 1, 39 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that the prior art did not disclose a training circuit including a finite state machine located on an integrated circuit (Remarks 4/20/2009; pages 12 -13). Examiner is using Ambrosio et al (US 4,755,984) to address this limitation.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 – 9, 11 – 14, 17 – 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation: "reduce the first signal" (lines 10 – 11). There is insufficient antecedent basis for this limitation in the claim.

Claims 2 – 9, 11 – 14, 17 – 30 are rejected based on their dependency on a rejected base claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3, 17, 35, 41, 42, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA) and further in view of Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984).

Regarding claim 1, Schneider discloses:

a path coupled between the transmitter and the receiver (signal path from output of "precoder" through "echo canceller" to output of the "front end");

a third signal from the input of the transmitter and to adjust the third signal in phase and amplitude to reduce the first signal at the output of the receiver buffer (signal path from output of "precoder" through "echo canceller" to output of the "front end"; Fig. 4, element "echo canceller" and output of the "front end"; column 8, lines 19 – 26; column 1, line 59 – column 2, line 19; wherein the third signal phase and amplitude being adjusted is interpreted as being done by the echo canceller);

Schneider does not disclose a differential buffer coupled between the transmitter buffer input and the receiver buffer output, where the buffer adjusts the third signal in amplitude and phase and that the training circuit, including a finite state machine, is located on an integrated circuit.

In the same field of endeavor, AAPA discloses an integrated circuit (Fig. 3 prior art) comprising:

a transmitter including a transmitter buffer input (Fig. 3, Die A, element 12; wherein the transmitter is on Die A transmitting a first signal via path 30 and 31 to Die B and the transmitter buffer is element 12);

a receiver including a receiver buffer output (Fig. 3, Die A receiver which receives a signal from Die B; receiver buffer 13 which is coupled to transmitter buffer 12).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the transmitter and receiver buffers of AAPA in Schneider's system because this would allow the echo canceller to be implemented using differential buffers Schneider's system.

In the same field of endeavor, however, Thomasson discloses a training circuit to set phase and amplitude characteristics of the differential buffer by determining which phase and amplitude characteristics minimize peak-to-peak noise at the receiver buffer output upon introduction of a training signal to the transmitter (Abstract; Fig 1; column 3, line 60 – column 5, line 50; wherein the minimization of peak-to-peak noise is done since Thomason's method tries to cancel out the echo by amplitude adjusting, inverting, and phase adjusting. It is obvious to one of ordinary skill in the art that these operations themselves would lead to the peak signal being minimized, even though Thomason may not explicitly say so).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Thomason in the system of Schneider because this would allow for the phase and amplitude characteristics to be determined for echo cancellation purposes.

In the same field of endeavor, however, Ambrosio discloses a training circuit including a finite state machine located on an integrated circuit (Fig. 2, shift register which generates the training pattern; column 2, lines 22 - 25; column 2, lines 15 – 16; wherein

the finite state machine is interpreted as the shift register). Ambrosio clearly discloses that his invention can be implemented on an integrated circuit.

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Ambrosio, in the system of Schneider because this would allow for implementation on an integrated circuit, thereby reducing cost and size.

Regarding claim 3, Schneider does not disclose the training circuit is configured to use a training pattern to vary the phase and amplitude characteristics of the buffer.

In the same field of endeavor, however, Ambrosio discloses the training circuit is configured to use a training pattern to vary the phase and amplitude characteristics of the buffer subsequent to power up or reset (Fig. 2, shift register which generates the training pattern; column 2, lines 22 - 25; column 2, lines 15 – 16; wherein the finite state machine is interpreted as the shift register).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Ambrosio, in the system of Schneider because this would allow for a training sequence to be sent, as is well known in the art.

Regarding claim 17, Schneider not discloses the finite state machine plus ADC generates a control voltage to vary the amplitude of the third signal.

In the same field of endeavor, however, Thomasson discloses an analog to digital converter coupled to the training circuit, wherein the analog to digital converter is configured to provide a control voltage to the differential buffer to vary an amplitude of the third signal (Fig. 1, element 41, output of element 42; column 2, lines 17 – 21; wherein the control voltage is interpreted as output of the subtractor 42 that is fed back to change the variable attenuator 41 which changes the amplitude of the echo replica signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Thomasson, in the system of Schneider because this would allow the amplitude of the echo replica signal to be controlled for echo cancellation, as is well known in the art.

Claim 35 is directed to method/steps of the same subject matter claimed in apparatus claim 1 and therefore, is rejected as explained in the rejection of claim 1 above.

Regarding claim 41, Schneider does not disclose the differential buffer is configured to said reduce the first signal at the receiver buffer output through a complete cancellation of the first signal at the receiver buffer output.

In the same field of endeavor, however, Thomasson discloses the differential buffer is configured to said reduce the first signal at the receiver buffer output through a complete cancellation of the first signal at the receiver buffer output (Abstract; Fig 1; column 3, line 60 – column 5, line 50; wherein the cancellation of the first signal at the

receiver buffer output is done since Thomason's method tries to cancel out the echo by amplitude adjusting, inverting, and phase adjusting).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Thomason in the system of Schneider because this would allow for the echo signal to be cancelled out, to eliminate it from entering the receiver.

Regarding claim 42, Schneider does not disclose training circuit is configured to set the phase and amplitude characteristics of the differential buffer by determination of which phase and amplitude characteristics minimize the peak-to-peak noise at the receiver buffer output.

In the same field of endeavor, however, Thomasson discloses to said reduce peak-to-peak noise, said training circuit is configured to set the phase and amplitude characteristics of the differential buffer by determination of which phase and amplitude characteristics minimize the peak-to-peak noise at the receiver buffer output (Abstract; Fig 1; column 3, line 60 – column 5, line 50; wherein the cancellation of the first signal at the receiver buffer output is done since Thomason's method tries to cancel out the echo by amplitude adjusting, inverting, and phase adjusting).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Thomason in the system of

Schneider because this would allow for the echo signal to be cancelled out, to eliminate it from entering the receiver.

Regarding claim 44, Schneider does not disclose a transmitter having a transmitter buffer including a transmitter buffer output and a transmitter buffer input.

In the same field of endeavor, AAPA discloses an integrated circuit (Fig. 3 prior art) comprising:

a transmitter configured to transmit a first signal to another integrated circuit, wherein the transmitter has a transmitter buffer including a transmitter buffer output and a transmitter buffer input (Fig. 3, Die A, element 12; wherein the transmitter is on Die A transmitting a first signal via path 30 and 31 to Die B and the transmitter buffer is element 12);

a receiver configured to receive a second signal from the other integrated circuit, wherein the receiver has a receiver buffer including a receiver buffer output and a receiver buffer input, and wherein the receiver buffer input is coupled to the transmitter buffer output (Fig. 3, Die A receiver which receives a signal from Die B; receiver buffer 13 which is coupled to transmitter buffer 12).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the transmitter and receiver buffers of AAPA in Schneider's system because this would allow the echo canceller to be implemented using differential buffers Schneider's system.

Regarding claim 45, Schneider discloses:

the differential buffer is configured to said cancel the first signal at the receiver buffer output through a complete cancellation of the first signal at the receiver buffer output (signal path from output of "precoder" through "echo canceller" to output of the "front end"; Fig. 4, element "echo canceller" and output of the "front end"; column 8, lines 19 – 26; column 1, line 59 – column 2, line 19; wherein cancellation of the first signal is interpreted as being done by the echo canceller);

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785), Ambrosio et al (US 4,755,984) as applied to claim 1 above, and further in view of Geist (US 6,362,672).

Regarding claim 2, Schneider does not disclose that the third signal is adjusted in rise time.

In the same field of endeavor, however, Geist discloses the differential buffer is further configured to adjust a rise time of the third signal (Abstract; Fig. 3; column 3, lines 36 – 51; wherein the third signal is interpreted as the signal A#40 that is adjusted to match the slope of the other signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the system of

Schneider because it would enable the two signals to be synchronized, thereby eliminating any off center crossing voltages, as disclosed by Geist (column 1, lines 32 – 45).

10. Claims 4, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to claim 1 and further in view of Adham et al. (US 6,100,716)

Regarding claim 4, Schneider does not disclose that the differential buffer is implemented as a chain of buffer stages.

In the same field of endeavor, however, Adham discloses the differential buffer is implemented as a chain of buffer stages (Fig. 5A; column 9, lines 7 – 21).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Adham, in the system of Schneider because this would allow the degraded signals to be restored after a few logic stages, as stated by Adham.

Regarding claim 6, Schneider does not disclose that the differential buffer has a variable current source.

In the same field of endeavor, however, Adham discloses the differential buffer has a variable current source to enable control of the amplitude or phase of the third signal

(column 5, line 59 – 67; column 6, lines 6 – 25; wherein setting the amplitude is interpreted as changing the voltage drop across the resistor).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Adham, in the system of Schneider because this would allow the output to be calculated utilizing the benefits of a differential buffer, namely reducing crosstalk, having a high SNR, as stated by Adham (column 6, lines 39 – 47).

11. Claims 7, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785), Ambrosio et al (US 4,755,984), as applied to claim 1 above, and further in view of Chang et al. (A CMOS Differential Buffer Amplifier with Accurate Gain and Clipping Control; July 1995, IEEE Journal of Solid State Circuits; pages 731 – 735).

Regarding claims 7, Schneider does not disclose varying a load of the differential buffer is varied by a finite state machine.

In the same field of endeavor, however, Chang discloses the programmable or variable load is set by means of a finite state machine to control amplitude or phase (page 731, 2nd column, 6 lines starting with "However, for modern digital telephone applications,

..."; wherein the finite state machine that controls the gain is interpreted as the external gain control).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Chang, in the system of Schneider because allowing the gain to be externally controlled would allow greater flexibility, as is well known in the art.

Regarding claim 38, Schneider does not disclose that the gain of the differential buffer is varied by a training pattern.

In the same field of endeavor, however, Chang discloses the gain of the differential buffer is varied by means of a finite state machine (page 731, 2nd column, 6 lines starting with "However, for modern digital telephone applications, ..."; wherein the finite state machine that controls the gain is interpreted as the external gain control).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Chang, in the system of Schneider because allowing the gain to be externally controlled would allow greater flexibility, as is well known in the art.

12. Claims 8, 11, 14, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to

claim 1 above, and further in view of Moore et al. (US 6,166,573), and Geist (US 6,362,672).

Regarding claim 8, Schneider does not disclose a coarse delay circuit, a fine delay circuit, an amplitude control circuit and a rise-time control circuit.

In the same field of endeavor, however, Moore discloses a coarse delay circuit and a fine delay circuit (Abstract; Fig. 1, elements 11, 12; column 1, lines 10 – 21; column 2, lines 5 – 21, 44 – 50).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Moore, in the system of Schneider because this would provide a means for adjusting the delay for echo cancellation, as disclosed by Moore (column 1, lines 10 – 21).

In the same field of endeavor, however, Thomasson discloses an amplitude control circuit (Abstract; Fig. 1, element 41; column 3, lines 60 – 65; column 5, lines 24 – 33).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Thomasson, in the system of Schneider because this would provide a means for adjusting the amplitude of the echo replica for echo cancellation, as disclosed by Thomasson.

In the same field of endeavor, however, Geist discloses a rise-time control circuit (Abstract; Fig. 3; column 1, lines 5 – 8; column 3, lines 36 – 51).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the system of Schneider because it would enable the two signals to be synchronized, thereby eliminating any off center crossing voltages, as disclosed by Geist (column 1, lines 32 – 45).

Regarding claim 11, Schneider does not disclose a coarse delay circuit comprising a digital delay line and control logic.

In the same field of endeavor, however, Moore discloses coarse delay circuit comprises digital delay line and control logic for controlling the multiplexers (Fig. 2; column 2, lines 51 – 67; wherein the control logic for controlling the multiplexers is interpreted as the control logic for the write pointer 16 and read pointer r_n).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Moore, in the system of Schneider because it would enable the delay to be controlled.

Regarding claim 14, Schneider does not disclose a finite state machine generates control signals from the digital delay line.

In the same field of endeavor, Moore discloses a finite state machine generates control signals to select the signals from the digital delay line in the coarse delay circuit varying a delay of the third signal with respect to the first signal (Fig. 2, elements 16 and r_n;

column 2, lines 51 – 67; wherein the controls signals that are generated to select delays from the delay line are interpreted as the read and write pointers).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Moore, in the system of Schneider because this would provide a means for selecting signals from the delay line.

Regarding claim 20, Schneider does not disclose the rise time control circuit comprises resistors, capacitors and switches.

In the same field of endeavor, Geist discloses the rise time control circuit comprises resistors, capacitors and switches (Abstract; Fig. 3, 5; column 3, lines 36 – 51; wherein the resistors and capacitors are as shown in Fig. 5).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the system of Schneider because this would provide a means for matching the rise times in the two signals.

13. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to claim 1 above, and further in view of Bellenger (US 6,320,867).

Regarding claim 9, Schneider does not disclose that during a calibration procedure the amplitude, phase and rise-time are adjusted during power or on request.

In the same field of endeavor, Bellenger discloses the phase and/or amplitude of the third signal is adjusted during a calibration procedure (column 27, lines 59 – column 29, line 3; wherein the third signal is interpreted as the echo replica, adjusting the phase/amplitude is interpreted obtaining the echo canceller coefficients using the training sequence).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Bellenger, in the system of Schneider because this would provide a means for training the echo canceller, as is well known in the art.

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereafter, AAPA) in view of Schneider (US 6,246,716), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to claim 1 above, and in view of Moore et al. (US 6,166,573), and Geist (US 6,362,672) as applied to claim 8 and 11 above, and further in view of Saeki (US 20020070783).

Regarding claim 12, the Schneider does not disclose that the digital delay line comprises a cascade of buffers.

In the same field of endeavor, however, Saeki discloses the digital delay line comprises a cascade of buffers (Fig. 18, element 14; page 1, paragraph 3).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Saeki, in the combined system described above because this would provide a means for storage of the signal, as is well known in the art.

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to claim 1 above, and further in view of Moore et al. (US 6,166,573), and Geist (US 6,362,672) as applied to claim 8 and 11 above, and further in view of Nourrcier (US 5,278,567).

Regarding claim 13, AAPA does not disclose a pair of multiplexers selects signals from a digital delay line.

In the same field of endeavor, however, Nourrcier discloses a pair of multiplexers selects signals from a digital delay line (Fig. 7; column 9, line 67 – column 10, line 24)..

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Nourrcier, in the system of Schneider because this would provide selecting the delay line signal, as is well known in the art.

16. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to claim 1 above, and further in view of Moore et al. (US 6,166,573), and Geist (US 6,362,672) as applied to claim 8 above, and further in view of Filliman et. al. (US 6,404,255).

Regarding claim 18, the Schneider does not disclose the amplitude control circuit comprises a buffer with variable load.

In the same field of endeavor, however, Filliman discloses the amplitude control circuit comprises a buffer with variable load (Fig. 7; column 6, line 42 – column 7, line 8).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Filliman, in the system of Schneider because this would allow the amplitude of the echo replica signal to be controlled for echo cancellation, as is well known in the art.

17. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to claim 1 above, and further in view of Moore et al. (US 6,166,573), and Geist (US 6,362,672) as

applied to claim 8 above, and further in view of Filliman et. al. (US 6,404,255) as applied to claim 18 above, and further in view of Marbot (US 5,334,891).

Regarding claim 19, Schneider does not disclose the transistors are NMOS transistors.

In the same field of endeavor, however, Marbot discloses the finite state machine is configured to control a gate voltage of an NMOS transistor to vary the variable load (Fig. 1; column 2, lines 10 – column 3, line 14).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the NMOS transistors, as taught by Marbot, in the system of Schneider because this would result in low power consumption , as is well known in the art.

18. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,246,716) in view of Applicant Admitted Prior Art (hereafter, AAPA), Thomasson (US 6,278,785) and Ambrosio et al (US 4,755,984) as applied to claim 1 above, and further in view of Moore et al. (US 6,166,573), and Geist (US 6,362,672) as applied to claim 8 above, and further in view of Julstrom (US 4,991,166).

Regarding claim 21, Schneider does not disclose that the rise time is controlled by the capacitor.

In the same field of endeavor, however, Julstrom discloses a finite state machine generates control signals to switch the capacitors in the rise-time control circuit to vary a the rise-time of the third signal (column 9, lines 49 – 63; wherein the rise time is controlled by the capacitors).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Julstrom, in the system of Schneider because this would allow the rise time to be adjusted.

19. Claims 39, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomasson (US 6,278,785) in view Minami US (4,977,551) and further Ambrosio et al (US 4,755,984).

Regarding claim 39, Thomasson discloses:
applying a training pattern to an input of a transmitter and determining a code that corresponds to a minimum noise condition; (Abstract; Fig 1; column 3, line 60 – column 5, line 50; wherein the minimization of peak-to-peak noise is done since Thomason's method tries to cancel out the echo by amplitude adjusting, inverting, and phase adjusting. It is obvious to one of ordinary skill in the art that these operations themselves would lead to the peak signal being minimized, even though Thomason may not explicitly say so).
Thomasson doesn't disclose applying a code to a DAC and that everything is on an integrated circuit.

In the same field of endeavor, however, Minami discloses varying a digital-to-analog code being applied to a digital-to-analog converter to adjust operating parameters of a differential buffer; measuring resulting noise conditions at an output buffer of a receiver coupled to an input buffer of the transmitter, wherein the noise conditions correspond to each applied digital-to- analog code; determining digital to analog code that corresponds to a minimum noise condition; applying the determined code to the digital to analog converter to calibrate the differential buffer.
(column 2, lines 35 – 49; Fig. 9).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Minami, in the system of Thomasson because it would enable the optimum amplitude and phase settings to be determined.

In the same field of endeavor, however, Ambrosio discloses a training circuit including a finite state machine located on an integrated circuit and all other transmitter and receiver components that are on an integrated circuit (Fig. 2, shift register which generates the training pattern; column 2, lines 22 - 25; column 2, lines 15 – 16; wherein the finite state machine is interpreted as the shift register). Ambrosio clearly discloses that his invention can be implemented on an integrated circuit.

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Ambrosio, in the system of

AAPA because this would allow for implementation on an integrated circuit, thereby reducing cost and size.

Claim 43 is similarly analyzed as the corresponding limitation in claim 39, since in the echo cancellation process, reducing the echo or the leakage signal will minimize it.

20. Claims 35 – 36, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomasson (US 6,278,785) in view Minami US (4,977,551) and further in view of Ambrosio et al (US 4,755,984) as applied to claim 39 above and further in view of AAPA.

Regarding claim 35, Thomasson discloses adjusting, via the differential buffer, the third signal in phase and amplitude; and coupling the adjusted third signal into the output buffer of the receiver to cancel a signal echo component of the second signal (Abstract; Fig 1; column 3, line 60 – column 5, line 50; wherein the minimization of peak-to-peak noise is done since Thomason's method tries to cancel out the echo by amplitude adjusting, inverting, and phase adjusting. It is obvious to one of ordinary skill in the art that these operations themselves would lead to the peak signal being minimized, even though Thomason may not explicitly say so).

Thomasson does not disclose transmitting a first signal from the output buffer of the transmitter to another circuit, wherein the first signal being is also coupled into an input buffer of the receiver; receiving a second signal from the other circuit;

transmitting a third signal from the input buffer of the transmitter through the differential buffer.

In the same field of endeavor, however, AAPA discloses a first signal from the output buffer of the transmitter to another circuit, wherein the first signal being is also coupled into an input buffer of the receiver; receiving a second signal from the other circuit; transmitting a third signal from the input buffer of the transmitter through the differential buffer (Fig. 3 prior art; Fig. 3, Die A, element 12; wherein the transmitter is on Die A transmitting a first signal via path 30 and 31 to Die B and the transmitter buffer is element 12; Fig. 3, Die A receiver which receives a signal from Die B; receiver buffer 13 which is coupled to transmitter buffer 12).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by AAPA, in the system of Thomasson because it would enable the echo to be cancelled.

Regarding claim 36, Thomasson discloses that the phase of the echo replica is opposite to the phase of the leakage signal (Abstract; Fig 1; column 3, line 60 – column 5, line 50; Thomason's method tries to cancel out the echo by amplitude adjusting, inverting, and phase adjusting).

Regarding claim 38, Thomasson discloses a gain property of the differential buffer is varied at least in part by using the training pattern (Abstract; Fig 1; column 3, line 60 – column 5, line 50; wherein the gain is set using the coarse and fine adjustments. The coarse and fine adjustments are interpreted as the training pattern).

21. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomasson (US 6,278,785) in view Minami US (4,977,551) and further in view of Ambrosio et al (US 4,755,984) as applied to claim 39 above and further in view of AAPA as applied to claim 35 above, and further in view of Geist (US 6,362,672).

Regarding claim 37, Thomasson does not disclose that the rise time of the third signal is adjusted to match the rise time of the first signal.

In the same field of endeavor, however, Geist discloses the rise time of the third signal applied to the output of the receiving buffer is adjusted to match the rise time of the first signal (Abstract; Fig. 3; column 3, lines 36 – 51; wherein the third signal is interpreted as the signal A#40 that is adjusted to match the slope of the other signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Geist, in the system of Thomasson because it would enable the two signals to be synchronized, thereby eliminating any off center crossing voltages, as disclosed by Geist (column 1, lines 32 – 45).

Allowable Subject Matter

22. Claims 5, 22 – 30, 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Prior Art Cited

23. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to echo cancellation and differential buffers/amplifiers:

Guidoux (US 4,621,173) discloses a method to reduce the convergence time of an echo canceller.

Ito et al. (US 5,450,457) discloses a sampling phase extracting circuit and echo canceller.

Mellado et al. (US 5,796,731) discloses multiline PCM interface for signal processing.

Shattil (US 20010019264) discloses a method and apparatus for a full-duplex electromagnetic transceiver

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADOLF DSOUZA whose telephone number is (571)272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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